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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,296	10/01/2002	Liang-Hua Lin	NAUP0477USA	5720

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,296	LIN ET AL.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,20 and 21* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submissions filed on 25 November 2004 have been entered.

Drawings

2. The drawings were received on 25 November 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 6, 8, 9, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,271,553 B1 (**Pan '533**) considered with the basic textbook, **Ghandi**, VLSI Fabrication

Principles, 2nd ed., John Wiley & Sons: New York, 1994, p. 393 for a showing of inherency for claim 8 only.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, **Pan '533** discloses a method of forming a photo sensor in a photo diode formed on a semiconductor wafer, a surface of the semiconductor **31** comprising a substrate **32** with first-type dopants, and an insulating layer **38** positioned on the surface of the substrate and surrounding the photo sensor (Figs. 2, 7, and 8), the method comprising:

forming a first mask layer (not shown) on the surface of the substrate **32** for defining positions of a plurality of first doped regions **44** distributed in the photo sensor **40** (col. 4, lines 26-41; note the first mask is implicitly present because it would be wholly impossible to form the regions **44** absent a mask blocking the regions not implanted);

performing a first ion implantation process utilizing second-type dopants to form the plurality of first doped regions **44** on the surface of the photo sensor **40** for increasing a contacting area between each first doped region and the substrate so as to increase a sensing area (col. 5, lines 1-5; Figs. 6-7; note there exists no requirement in the claim that the "first doped regions" be isolated first each other, so the first doped regions **44** are taken to be each side of the rectangle at the perimeter of the photo sensor **40**);

removing the first mask layer and forming a second mask layer (not shown) surrounding the photo sensor (col. 4, lines 26-41; note the second mask is implicitly present because it would be wholly impossible to form the regions **42** absent a mask blocking the regions not implanted); and

performing a second ion implantation process utilizing second-type dopants to form a second doped region **42** on the surface of the photo sensor, and the second doped region **42** being overlapped with a partial region of each of the first doped regions **44** (col. 4, lines 26-41; overlapping is shown to occur at the edges of the regions **42** and **44** in Figs. 2 and 7).

Note also that at col. 3, line 58 to col. 4, line 15, **Pan '533** teaches the necessity of masks for implantation. This provides additional evidence of the implicit use of the first and second masks.

Note also **Pan '533** suggests at col. 4, lines 41-47,

> "In addition, the order of the ion implantation processes for the n-type doped regions **42** and **44** could also be exchanged." (Emphasis added.)

Accordingly, the order of the first and second masks can be interchanged.

Regarding claim 2, **Pan '533** discloses the method of claim 1 wherein the dopants in the first doped regions **44** and in the second doped region **42** interact with neighboring substrate **32** to form a plurality of depletion regions (Fig. 2. Compare to instant Figs. 5 and 6, which show the depletion regions to be contiguous.)

Regarding claim 3, **Pan '533** discloses the method of claim 1 wherein the first-type dopants are N-type, and the second-type dopants are P-type (col. 3, lines 39-44).

Regarding claim 4, **Pan '533** discloses the method of claim 1 wherein the first-type dopants are P-type, and the second-type dopants are N-type (col. 3, line 49; col. 4, lines 26-41).

Regarding claim 6, **Pan '533** discloses the method of claim 1 wherein a dopant density of the first ion implantation process is less than a dopant density of the second ion implantation process (col. 3, lines 29-38).

Regarding claim 8, the method of claim 1 further inherently comprises an annealing process for driving-in the dopants in the second doped region in order to activate the dopants as taught to be essential in **Ghandi** at p. 393.

Regarding claim 9, **Pan '533** discloses the method of claim 1 wherein each of the depletion regions formed between the neighboring first doped regions is inherently a complete depletion region, and a capacitance of each of the depletion regions is approximately equal to zero for increasing a sensing area, decreasing dark current, and further increasing photo current and photon conversion gain as admitted by Applicant in the instant specification because the **Pan** structure is the same structure **as presently claimed**. (See MPEP 2112.)

Regarding claim 20, **Pan '533** discloses the method of claim 1 wherein the first mask layer and the second mask layer further define positions for forming a plurality of depletion regions in the photo sensor, each of the depletion regions being located under the second doped region **42**, between the two adjacent first doped regions **44**, and extending under the two adjacent first doped regions **44**, **as shown in Fig. 2**.

5. Claims 1, 2, 4, 5, 7, 8-10, 20, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,150,189 (**Pan '189**) considered with the basic textbook, **Ghandi**, VLSI Fabrication Principles, 2nd ed., John Wiley & Sons: New York, 1994, p. 393 for a showing of inherency for claim 8 only.

Regarding independent claims 1 and 21, **Pan '189** discloses a method of forming a photo sensor in a photo diode formed on a semiconductor wafer, a surface of the semiconductor comprising a substrate **22** with first-type dopants (col. 3, line 1), and an insulating layer **32** positioned on the surface of the substrate and surrounding the photo sensor (Figs. 2-6; col. 3, lines 50-54), the method comprising:

forming a first mask layer (not shown) on the surface of the substrate **22** for defining positions of a plurality of first doped regions **28** distributed in the photo sensor (col. 3, lines 12-18; note the first mask is implicitly present because it would be wholly impossible to form the regions **28** absent a mask blocking the regions not implanted);

performing a first ion implantation process utilizing second-type dopants to form the plurality of first doped regions **28** on the surface of the photo sensor for increasing a contacting area between each first doped region and the substrate so as to inherently increase a sensing area (col. 3, lines 12-18 and especially the paragraph bridging cols. 3-4 and col. 4, lines 38-41);

removing the first mask layer and forming a second mask layer **40** surrounding the photo sensor (Fig. 5); and

performing a second ion implantation process utilizing second-type dopants to form a second doped region **42** on the surface of the photo sensor, and the second doped region **42** being overlapped with a partial region of each of the first doped regions **28** (Figs. 5 and 6; col. 3, lines 42-45).

Regarding claim 2, **Pan '189** discloses the method of claim 1 wherein the dopants in the first doped regions **28** and in the second doped region **42** interact with neighboring substrate **22**

to form a plurality of depletion regions. (Fig. 6. Compare to instant Figs. 5 and 6, which show the depletion regions to be contiguous.)

Regarding claim 4, **Pan '189** discloses the method of claim 1 wherein the first-type dopants are P-type, and the second-type dopants are N-type (col. 3, line 1 and lines 33-47).

Regarding claim 5, **Pan '189** discloses the method of claim 1 wherein the substrate **22** further comprises an epitaxial silicon layer, and each of the first doped regions and the second doped region are formed inside the epitaxial silicon layer (col. 3, first paragraph).

Regarding claim 7 and further regarding claim 21, **Pan '189** discloses method of claim 1 wherein the surface of the semiconductor wafer further comprises a logic circuit region, and the second ion implantation process forms at least a lightly doped drain (LDD) **46** within the logic circuit region (col. 3, lines 45-48). Note that the term "lightly doped" is a relative term of degree without bounds. Accordingly, any doping amount of the **Pan '189** drain **46** may be taken to be "lightly doped."

Regarding claim 8, the method of claim 1 further inherently comprises an annealing process for driving-in the dopants in the second doped region in order to activate the dopants as taught to be essential in **Ghandi** at p. 393.

Regarding claim 9, **Pan '189** discloses the method of claim 1 wherein each of the depletion regions formed between the neighboring first doped regions is inherently a complete depletion region, and a capacitance of each of the depletion regions is approximately equal to zero for increasing a sensing area, decreasing dark current, and further increasing photo current and photon conversion gain as admitted by Applicant in the instant specification because the **Pan** structure is the same structure **as presently claimed**. (See MPEP 2112.)

Regarding claim 10, **Pan '189** discloses the method of claim 1 wherein the second doped region **42** is capable of being utilized as a conducting wire of the photo sensor (col. 3, lines 42-48; col. 4, lines 17-21).

Regarding claim 20, **Pan '189** discloses the method of claim 1 wherein the first mask layer and the second mask layer **40** further define positions for forming a plurality of depletion regions in the photo sensor, each of the depletion regions being located under the second doped region **42**, between the two adjacent first doped regions **28**, and extending under the two adjacent first doped regions **28**, **as shown in Fig. 6**.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7 and 21 are rejected under 35 U.S.C. 103(a) as being obvious over **Pan '533**.

Applicant has NOT provided evidence in this file showing that the invention was owned by, or subject to an obligation of assignment to, the same entity as **Pan '533** at the time this invention was made. In the event Applicant so does, **Pan '533** would be is disqualified as prior art through 35 U.S.C. 102(e), (f) or (g) in any rejection under 35 U.S.C. 103(a) in this application. However, this applied art additionally qualifies as prior art under another subsection of 35 U.S.C. 102 and accordingly is **not disqualified** as prior art under 35 U.S.C. 103(a).

Applicant may overcome the applied art either by a showing under 37 CFR 1.132 that the invention disclosed therein was derived from the inventor of this application, and is therefore, not the invention "by another", or by antedating the applied art under 37 CFR 1.131.

Regarding claims 7 and 21, the prior art of **Pan '533**, as explained above, discloses each of the claimed features except for indicating that the second mask is also used to form a light-doped drain (LDD). **Pan '533** does, however suggest at col. 4, lines 41-47,

> "Although in the above description the **NMOS transistor 36** is formed before **the photo sensor 40**, the processing order of **the two devices** could be swapped, or they **could be formed together simultaneously**. In addition, the order of the ion implantation processes for the n-type doped regions **42** and **44** could also be exchanged." (Emphasis added.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the LDD of the NMOS simultaneously with the formation of the second region **42** of **Pan '533** to consolidate processing which saves money by consolidating reticles and saves time and money by consolidating otherwise separate photoresist deposition, patterning, repair, cleaning, etcetera, into one implantation processing cycle.

8. Claims 1-5, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,767,538 (**Mullins** et al.) in view of **Van Zant**, Microchip Fabrication, 4th ed. McGraw-Hill: New York, 2000, pp. 72-74.

Regarding claim 1, **Mullins** discloses a method of forming a photo sensor **5** (Fig. 3A) in a photo diode **5** formed on a semiconductor wafer **50**, a surface of the semiconductor comprising a substrate with first-type dopants, and an insulating layer positioned on the surface of the substrate and surrounding the photo sensor **5**, the method comprising:

performing a first ion implantation process utilizing second-type dopants to form the plurality of first doped regions **47** distributed in the photo sensor **5** thereby shown to increase a contacting area between each first doped region and the substrate so as to inherently increase a sensing area;

performing a second ion implantation process utilizing second-type dopants to form a second doped region **46** on the surface of the photo sensor **5**, and the second doped region being overlapped with a partial region of each of the first doped regions (Fig. 3A; col. 8, line 66 to col. 9, line 26).

Mullins does not teach that first and second masks are used to perform the first and second implantations to form the separate doped regions **46** and **47**.

Van Zant teaches that it is essential to use a patterned mask having windows formed over regions of the substrate in which ions are to be implanted while blocking the remaining regions in which no ions are to be implanted.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use first and second masks in **Mullins** to implant the separate areas **46** and **47** because the regions has different profiles and therefore require separate implantation steps, as taught by **Van Zant** to be essential.

Regarding claim 2, **Mullins** discloses the method of claim 1 wherein the dopants in the first doped regions and in the second doped region interact with neighboring substrate to form a plurality of depletion regions (Fig. 3A).

Regarding claim 3, **Mullins** discloses the method of claim 1 wherein the first-type dopants are N-type, and the second-type dopants are P-type (Fig. 3A).

Regarding claim 4, **Mullins** discloses the method of claim 1 wherein the first-type dopants are P-type, and the second-type dopants are N-type (col. 11, lines 7-10).

Regarding claim 5, **Mullins** discloses the method of claim 1 wherein the substrate further comprises an epitaxial silicon layer, and each of the first doped regions and the second doped region are formed inside the epitaxial silicon layer (col. 4, lines 30-33).

Regarding claim 8, **Mullins** discloses the method of claim 1 wherein the method further comprises an annealing process for driving-in the dopants in the second doped region.

Regarding claim 9, **Mullins** discloses the method of claim 1 wherein each of the depletion regions formed between the neighboring first doped regions is inherently a complete depletion region, and a capacitance of each of the depletion regions is approximately equal to zero for increasing a sensing area, decreasing dark current, and further increasing photo current and photon conversion gain as admitted by Applicant in the instant specification because the **Mullins** structure is the same structure as presently claimed. (See MPEP 2112.)

Regarding claim 10, the method of claim 1 wherein the second doped region **46** is utilized to be a conducting wire of the photo sensor (Fig. 3A).

Response to Arguments

9. Applicant's arguments filed 25 November 2004 have been fully considered but they are not fully persuasive.

Applicant's amendments to the claims combined with the arguments of record overcome the rejection over Kagawa.

In response to applicant's arguments against the Mullins and Van Zant references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, Mullins teaches the implantation steps and Van Zant teaches the necessity of masks to block implantation into regions where implantation is not desired. Accordingly, the combination is proper and makes obvious the use of the first and second masks in Mullins.

Applicant has contended that Examiner characterized the first doped region 47 in Mullins as the contacting wire. Examiner did not. As clearly stated in the previous and present Office actions the second doped region 46 also serves as a conducting wire.

Note also the Mullins in not required to recognize or discuss the increase in contacting area by performing plural first implanted regions. Note Tthe claiming of a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable. See *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977). Anticipation by a prior art reference does not require either the inventive concept of the claimed subject matter or the recognition of inherent properties that may be possessed by the prior art reference. See *Verdegaal Bros. Inc. v. Union Oil Co.*, 814 F.2d 628, 633, 2 USPQ2d 1051, 1054 (Fed. Cir.), cert. denied, 484 U.S. 827 (1987). A prior art reference anticipates the subject matter of a claim when the reference discloses every feature of the claimed invention, either explicitly or inherently. See *Hazani v. Int' l Trade Comm'n*, 126 F.3d 1473, 1477, 44 USPQ2d 1358, 1351 (Fed. Cir. 1997) and *RCA Corp. v. Applied Digital Data Systems, Inc.*, 730 F.2d 1440, 14.44, 221 USPQ 385, 388 (Fed. Cir. 1984). The law of anticipation does not require that the reference

teach what the appellants are claiming, but only that the claims on appeal "read on" something disclosed in the reference. See *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 772, 218 CSPQ 781, 789 (Fed. Cir. 1'983), cert. denied, 465 U.S. 1026 (1984).

Accordingly, the arguments are not persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached from 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erik Kielin
Primary Examiner
February 12, 2005